FIG. 1

(method of generating test sequence for delay fault)

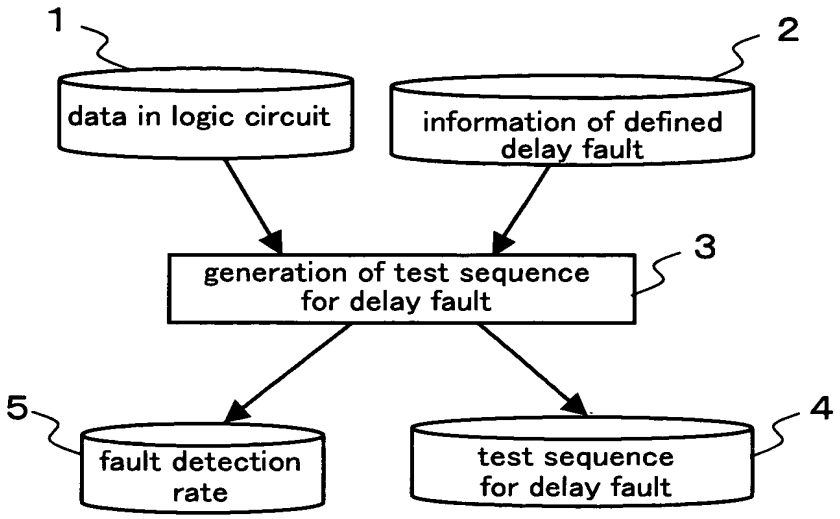

FIG. 2

(method of simulating delay fault)

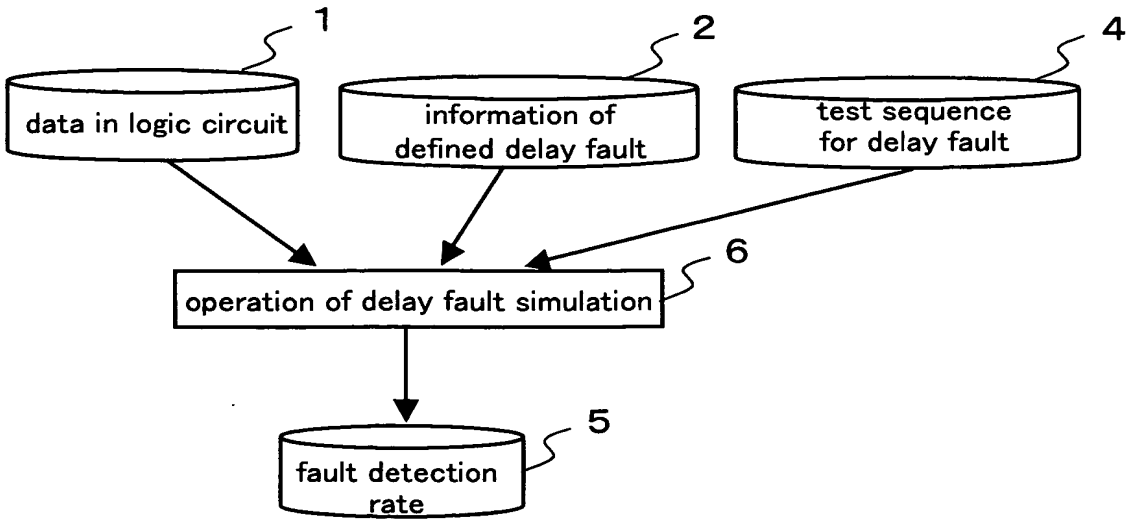

FIG. 3

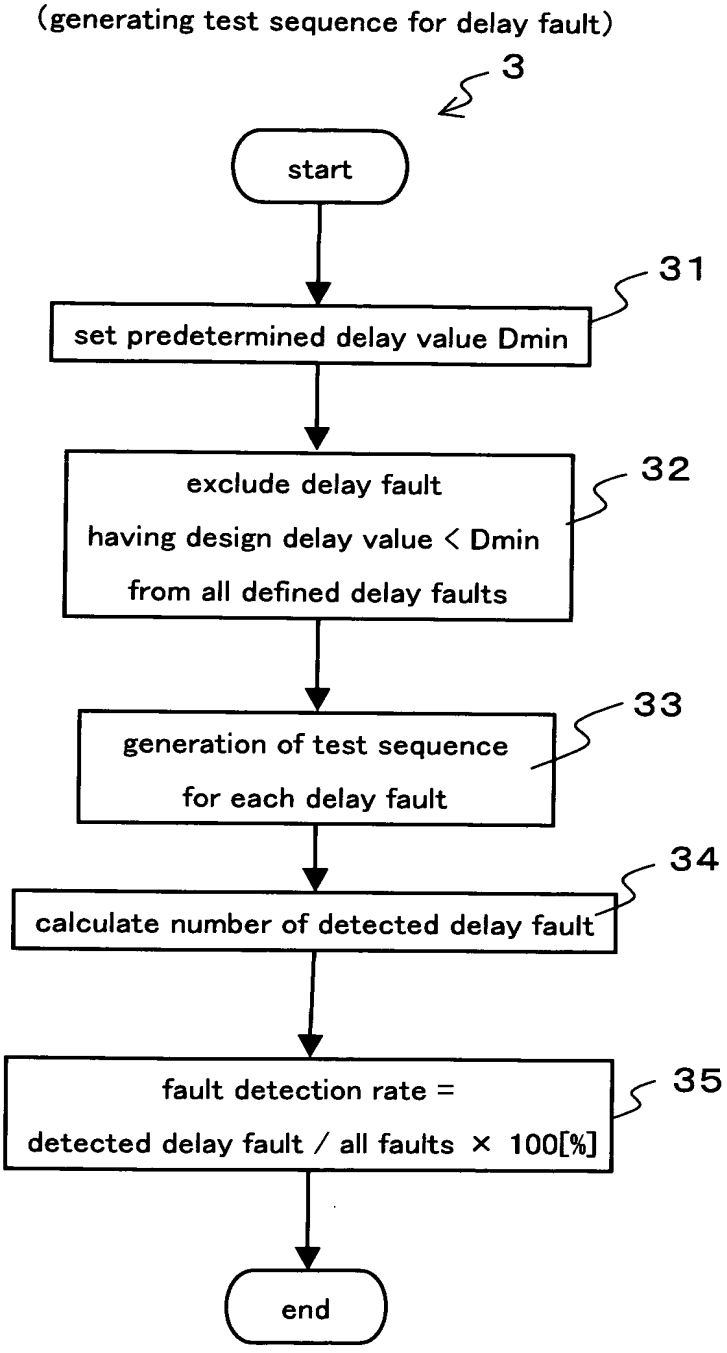
(generating test sequence for delay fault)
3
start
31
set predetermined delay value Dmin
32
exclude delay fault
having design delay value < Dmin
from all defined delay faults
33
generation of test sequence
for each delay fault
34
calculate number of detected delay fault
35
fault detection rate =
detected delay fault / all faults × 100[%]
end

FIG. 4

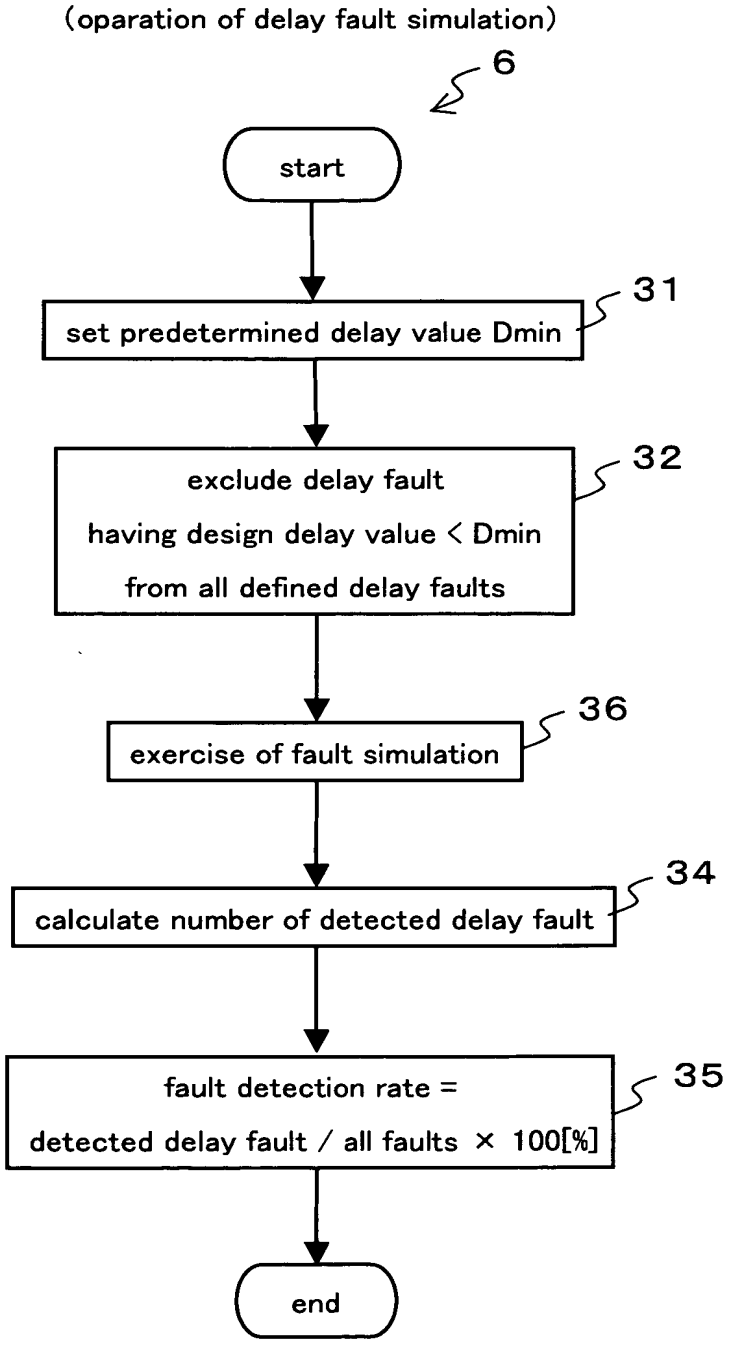
(oparation of delay fault simulation)
6
start
31
set predetermined delay value Dmin
32
exclude delay fault
having design delay value < Dmin
from all defined delay faults
36
exercise of fault simulation
34
calculate number of detected delay fault
35
fault detection rate =
detected delay fault / all faults × 100[%]
end

FIG. 5

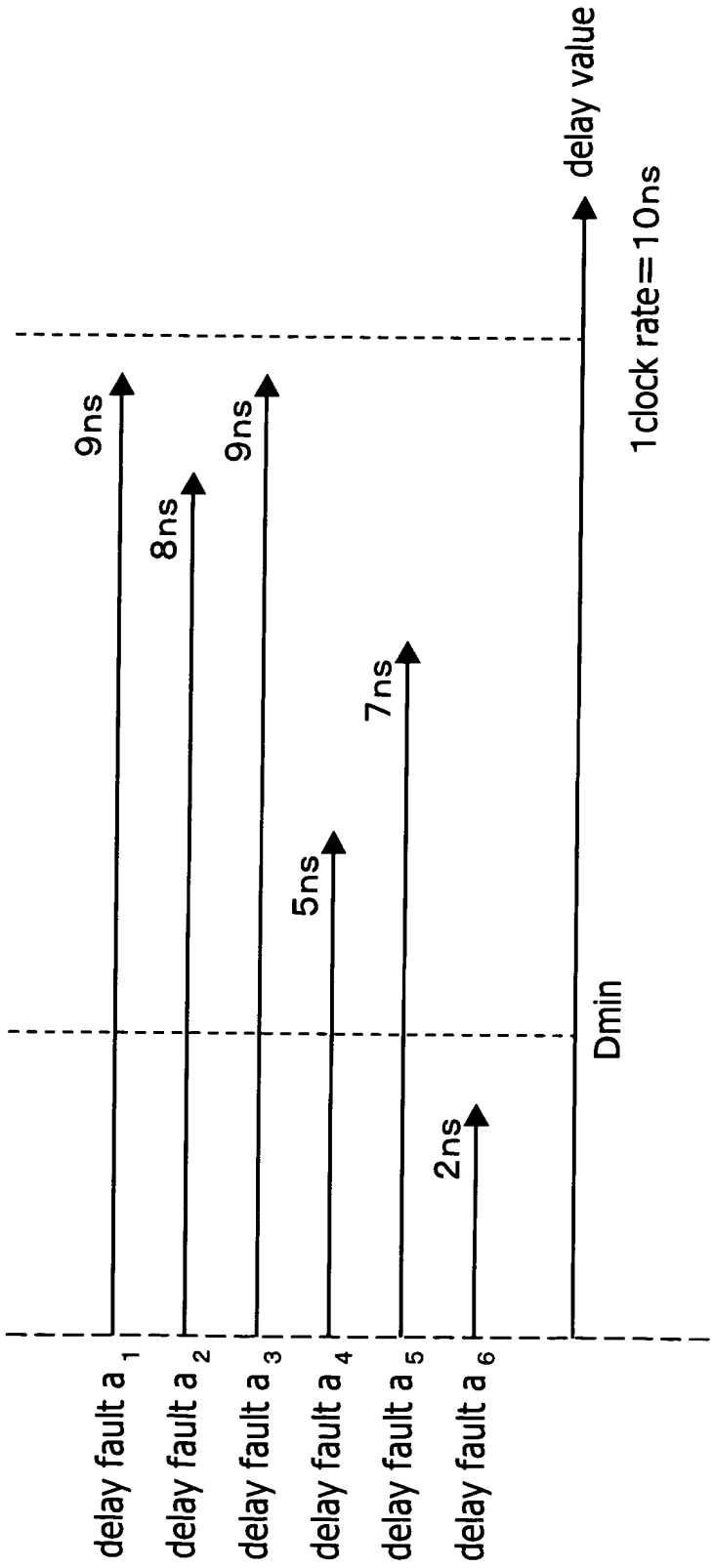
delay value
1clock rate=10ns
9ns
8ns
9ns
5ns
7ns
2ns
Dmin
delay fault a 1
delay fault a 2
delay fault a 3
delay fault a 4
delay fault a 5
delay fault a 6

FIG. 6

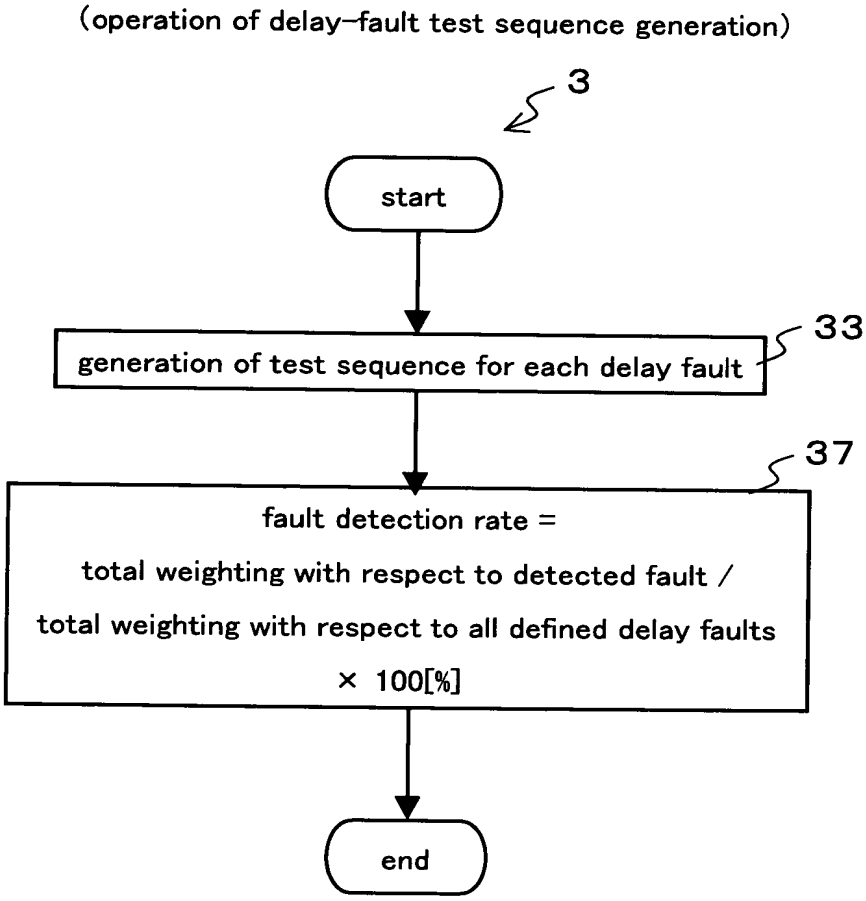
(operation of delay-fault test sequence generation)
3
start
generation of test sequence for each delay fault
33
37
fault detection rate =
total weighting with respect to detected fault /
total weighting with respect to all defined delay faults
× 100[%]
end

FIG. 7

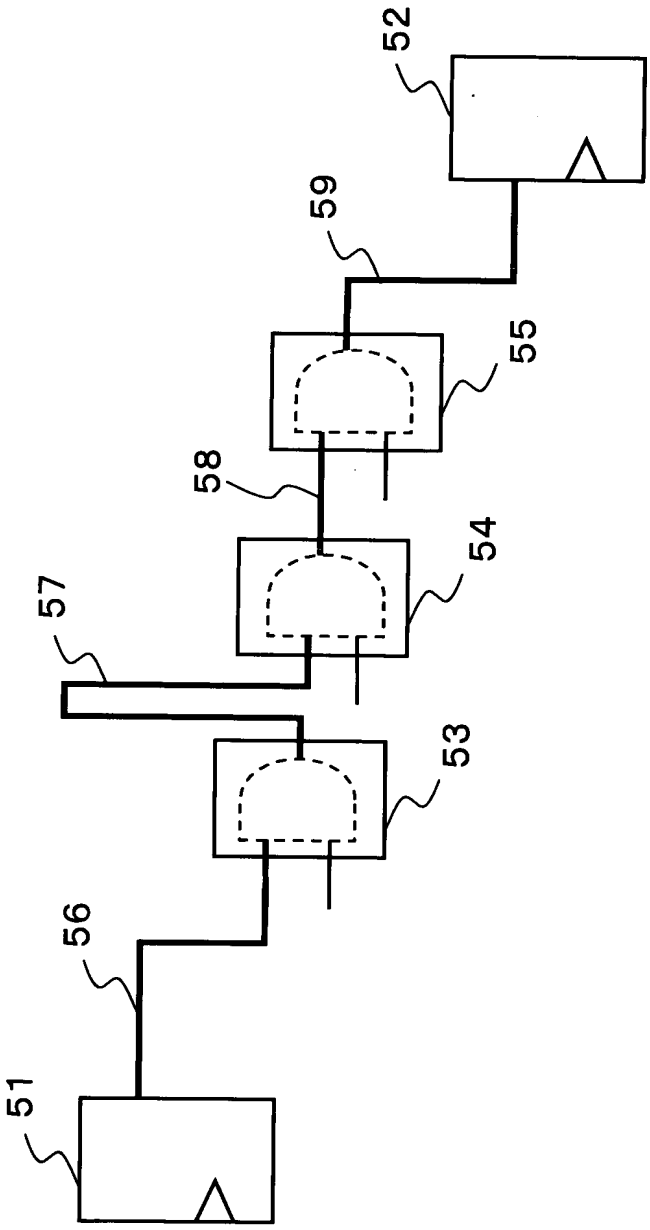

FIG. 8

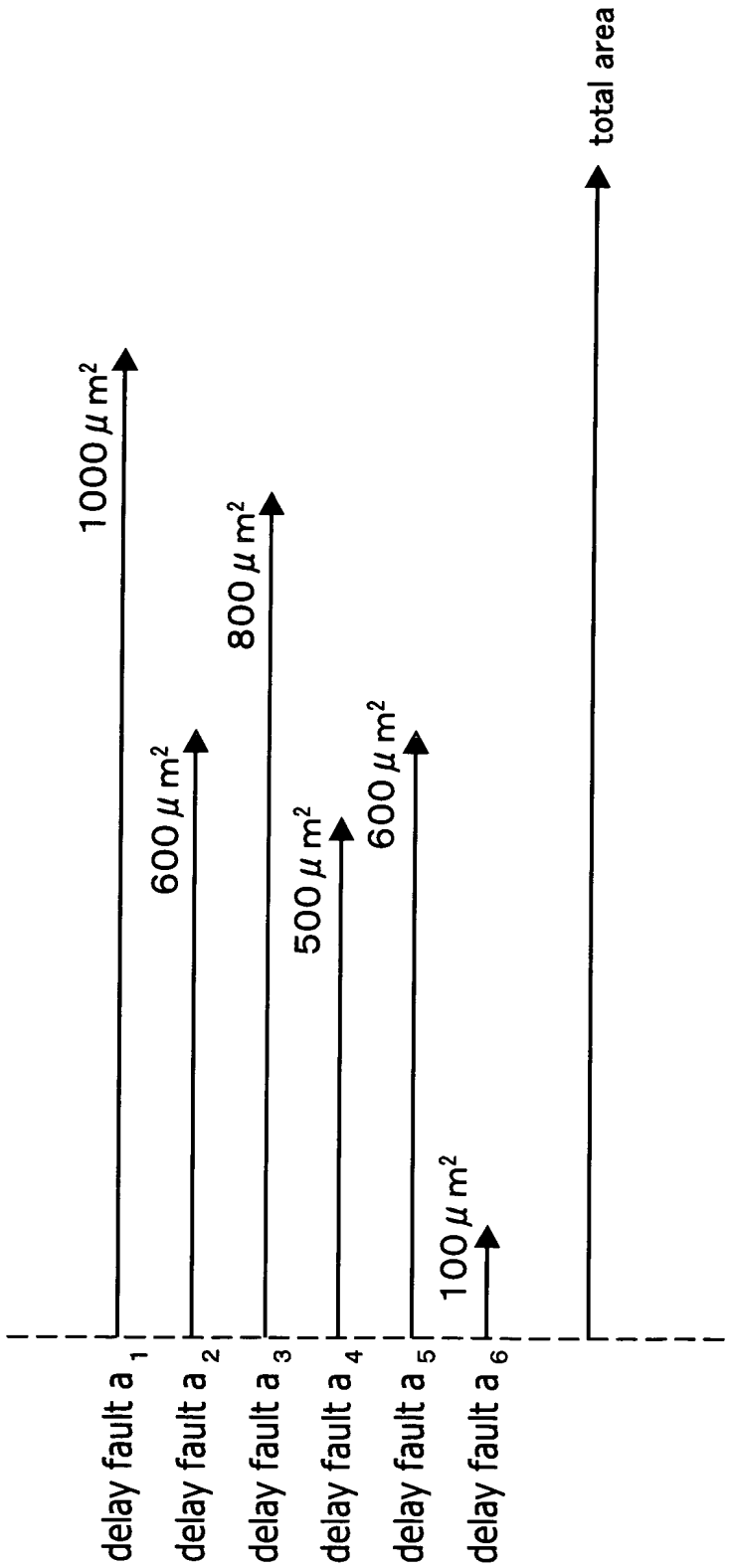
1000 μm²
600 μm²
800 μm²
500 μm²
600 μm²
100 μm²
total area
delay fault a 1
delay fault a 2
delay fault a 3
delay fault a 4
delay fault a 5
delay fault a 6

FIG. 9

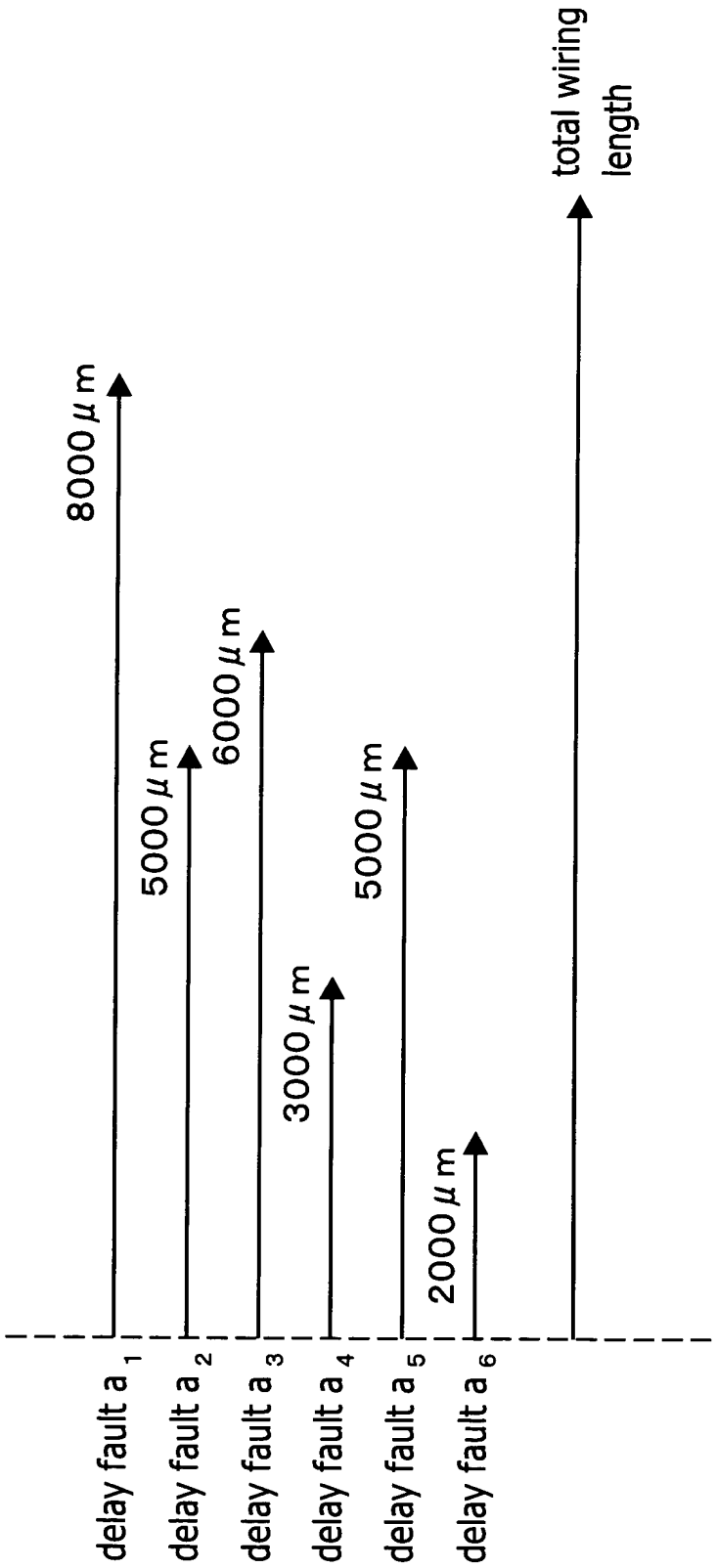
8000 μm
5000 μm
6000 μm
3000 μm
5000 μm
2000 μm
total wiring length
delay fault a 1
delay fault a 2
delay fault a 3
delay fault a 4
delay fault a 5
delay fault a 6

FIG. 10

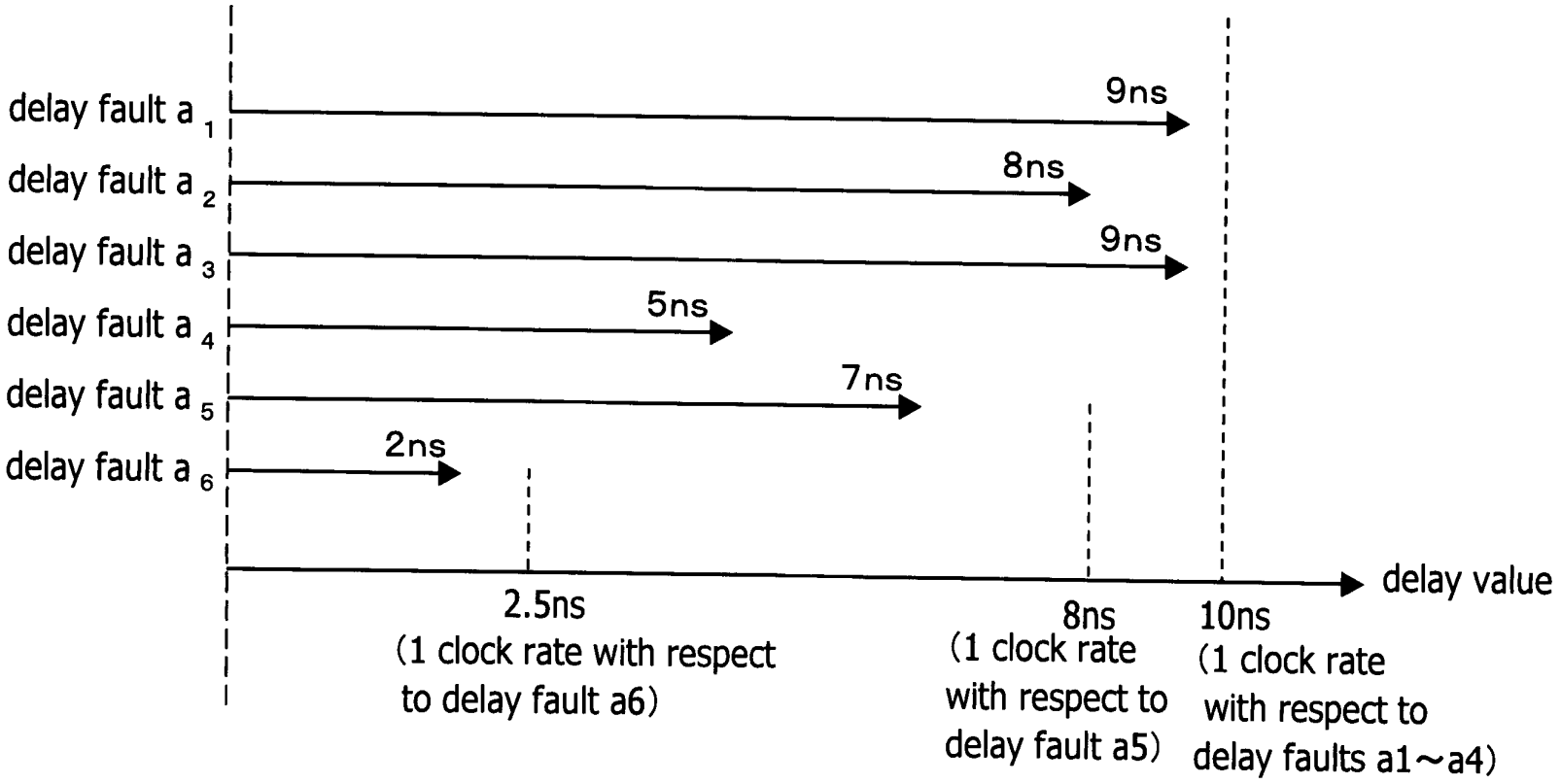
delay fault a 1
delay fault a 2
delay fault a 3
delay fault a 4
delay fault a 5
delay fault a 6
9ns
8ns
9ns
5ns
7ns
2ns
delay value
2.5ns
(1 clock rate with respect to delay fault a6)
8ns
(1 clock rate with respect to delay fault a5)
10ns
(1 clock rate with respect to delay faults a1～a4)

FIG. 11

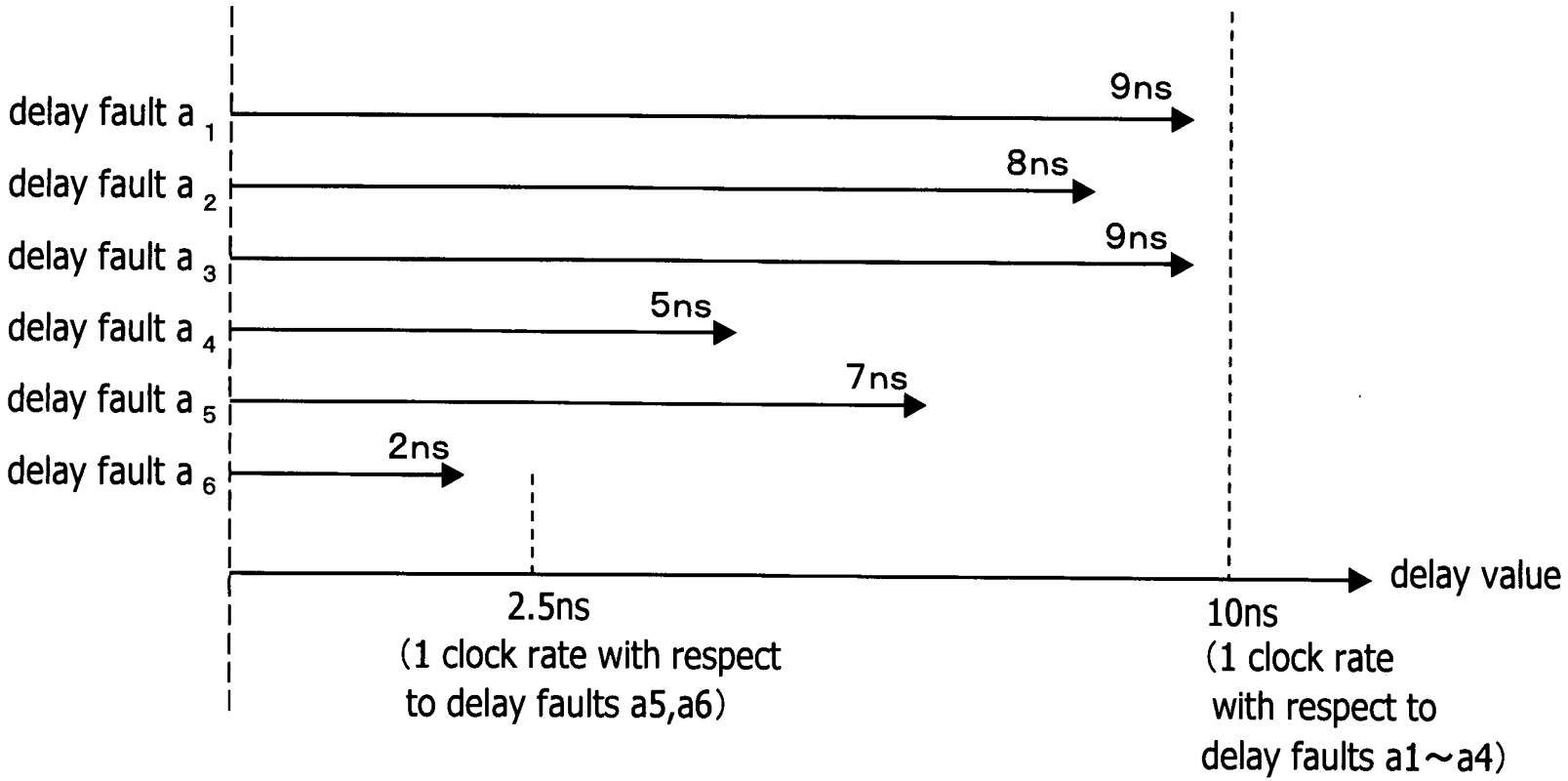
delay fault a 1
delay fault a 2
delay fault a 3
delay fault a 4
delay fault a 5
delay fault a 6
9ns
8ns
9ns
5ns
7ns
2ns
delay value
2.5ns
(1 clock rate with respect to delay faults a5,a6)
10ns
(1 clock rate with respect to delay faults a1~a4)

FIG. 12

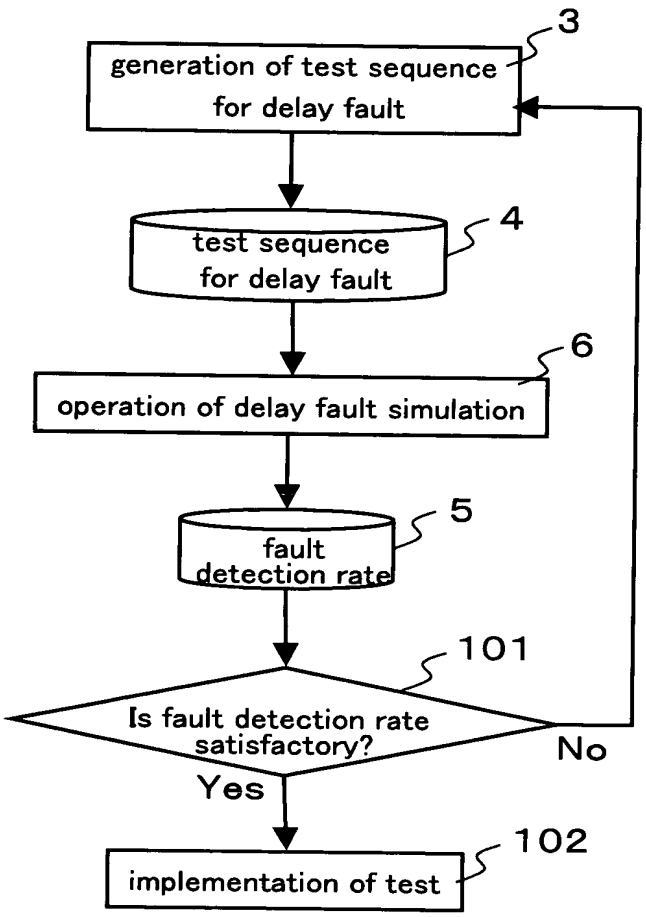
3
generation of test sequence for delay fault
4
test sequence for delay fault
6
operation of delay fault simulation
5
fault detection rate
101
Is fault detection rate satisfactory?
No
Yes
102
implementation of test

FIG. 13 PRIOR ART

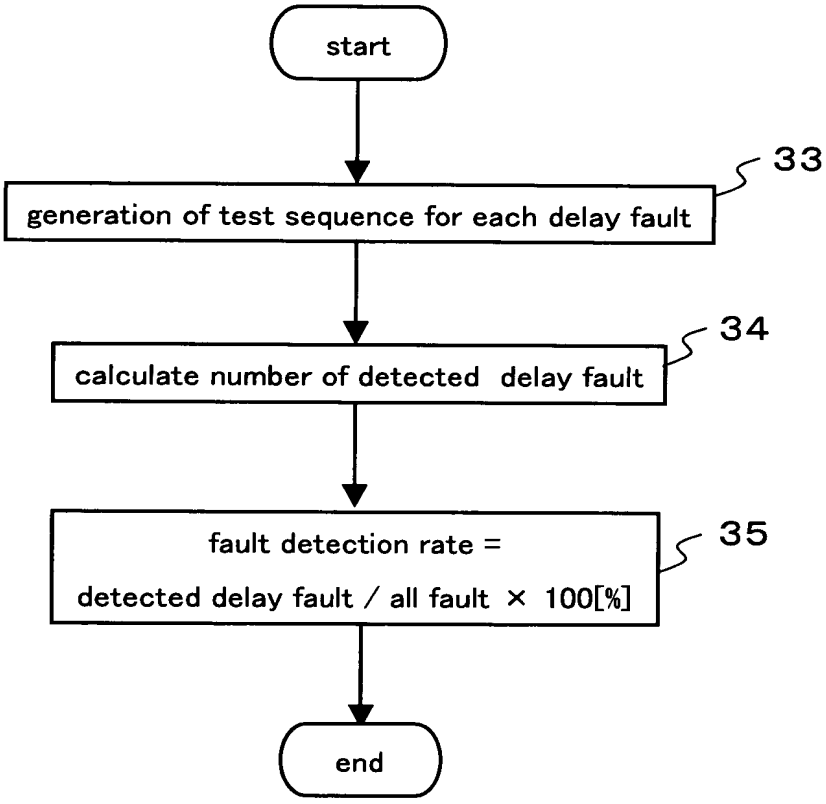

FIG. 14 PRIOR ART